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Serial No. 10/618,041

Application of: Lee A. Burton

Filed: July 11, 2003

Art Unit:

Examiner:

Attorney Docket No. SRC027

For: SWITCH/NETWORK ADAPTER PORT INCORPORATING SHARED MEMORY RESOURCES SELECTIVELY ACCESSIBLE BY A DIRECT EXECUTION LOGIC ELEMENT AND ONE OR MORE DENSE LOGIC DEVICES

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In re Application of:
Lee A. Burton
Serial No. 10/618,041
Filed: July 11, 2003
For: SWITCH/NETWORK ADAPTER PORT INCORPORATING SHARED MEMORY RESOURCES SELECTIVELY ACCESSIBLE BY A DIRECT EXECUTION LOGIC ELEMENT AND ONE OR MORE DENSE LOGIC DEVICES

Confirmation No.:
Group Art Unit:
Examiner:

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This Information Disclosure Statement is filed before mailing of a first Office Action in the above case. Accordingly, no fee is believed due. However, any fee associated herewith may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

12 December 2003
Date

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Sheet	1	of	5	Attorney Docket No.	SRC027

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.[1]	Document No. No. – Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines, Where Relavant Passages or Relevant Figures Appear
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		YAMAUCHI, TSUKASA, et al., "SOP: A reconfigurable massively parallel system and its control-data flow based compiling method", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 148-156.	
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